WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a comparator comparing a value of data read from each memory cell connected to an activated word line with an expected value to be read from said each memory cell, for each column in a test mode; and

an error register accumulatively holding error data based on a comparison result by said comparator, wherein

each bit of said error data indicates said comparison result by said comparator for a corresponding column, and

said each bit takes a first logical value when said comparison result for said corresponding column always indicates equality whichever word line is activated, and takes a second logical value when once said comparison result for said corresponding column indicates difference.

2. The semiconductor integrated circuit according to claim 1, wherein

said semiconductor integrated circuit has a plurality of modules connected to a common internal data bus, and performing reading operations from memory cells simultaneously in the test mode, and

said each module includes a switch circuit prohibiting data read from a memory cell from being output to the internal data bus in the test mode.

3. The semiconductor integrated circuit according to claim 1, wherein

said semiconductor integrated circuit has a plurality of modules having their operations controlled by respective chip select signals, and

said each module has a control circuit controlling an operation of reading or writing data from or into a memory cell, irrespective of a value of said chip select signal, in the test mode.

4. The semiconductor integrated circuit according to claim 3,

wherein

said plurality of modules receive a common address signal sent through a common internal address bus, where said plurality of modules have word lines different in number,

said control circuit in a module that does not have a maximum number of word lines controls an operation of reading or writing data from or to a memory cell, irrespective of a value of said chip select signal, only when values of one or more prescribed bits forming an address signal are prescribed values, and

said prescribed bits are used in specifying a word line of a module having a maximum number of word lines and are not used in specifying a word line of said module that does not have a maximum number of word lines.

5. The semiconductor integrated circuit according to claim 1, wherein

said semiconductor integrated circuit has a plurality of banks receiving a common address signal and having their operations controlled by one or more bits forming said address signal, and

said each bank includes a control circuit controlling an operation of reading or writing data from or into a memory cell, irrespective of values of said one or more bits forming an address signal controlling said operation.

6. The semiconductor integrated circuit according to claim 1, wherein said semiconductor integrated circuit has a redundancy circuit in a column.

7. The semiconductor integrated circuit according to claim 6, wherein said error register outputs held error data when an address signal indicates a prescribed value,

said semiconductor integrated circuit further comprising a repair code generation circuit receiving said error data for generating a repair code for repairing a defective memory cell array using said redundancy circuit.

8. The semiconductor integrated circuit according to claim 7 comprising:

a program circuit including at least one fuse element for outputting a repair code corresponding to a state of said fuse element;

a register holding a repair code;

a selector selecting and outputting one of the repair code output from said program circuit and the repair code output from said register; and

a repair control circuit controlling repair of a defective memory cell array in accordance with the repair code output from said selector.

9. The semiconductor integrated circuit according to claim 6 comprising:

a program circuit including at least one fuse element for outputting a repair code corresponding to a state of said fuse element;

a register holding a repair code;

a selector selecting and outputting one of the repair code output from said program circuit and the repair code output from said register;

a repair control circuit controlling repair of a defective memory cell array in accordance with the repair code output from said selector; and

a processor controlling an execution of a two-step test, wherein

said processor controls writing of test data into a memory cell and reading of test data from a memory cell without causing said repair control circuit to perform repair in a first step of the test,

generates a repair code corresponding to error data stored in said error register in said first step of the test for storage into said register, and

controls writing of test data into a memory cell and reading of test data from a memory cell while allowing said selector to output the repair code from said register to cause said repair control circuit to perform the repair.